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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,787	03/17/2004	Eitan Cadouri	524322001100	8052

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EXAMINER	
WACHSMAN, HAL D	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 06/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/803,787	CADOURI, EITAN	
	Examiner	Art Unit	
	Hal D. Wachsman	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-18* is/are allowed.

6)☒ Claim(s) *1,2 and 19* is/are rejected.

7)☒ Claim(s) *3-10 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The drawings are objected to because labeling is needed in Figure 1 of components 104, 106 and 108 so as to facilitate an understanding of the invention from the drawing. Appropriate correction is required.

2. The Examiner respectfully notes the following grammatical errors in the specification: paragraph 0004 "reparable" and paragraph 0019 "in particular*ly*".

3. Paragraph 0019 of the specification defines the actual yield value as a ratio of the number of *particular* ICs or portions of an IC that passed the one or more tests and a total number of *particular* ICs or portions of an IC tested. Paragraph 0022 of the specification then defines the average yield value as a ratio of the number of the *plurality* of ICs or portions of an IC that passed the one or more tests and a total number of the *plurality* of ICs or portions of an IC tested. As particular ICs are also a plurality of ICs and it is possible for the particular ICs to be the total number of the plurality of ICs, there is some confusion therefore what distinguishes then the average yield value ratio determination from the actual yield value ratio determination. Appropriate correction is required.

4. Claims 1-20 are objected to under 37 C.F.R. 1.75(a) for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. The preamble of claim 1 cites "A method for producing publishable yield information.." however the body of the claim does not particularly point out how the generation of the transformed yield value results in publishable yield information. In addition, the generating a transformed yield value step does not particularly point out how exactly the actual yield value and the average yield value are used to generate a

transformed yield value. Claim 2 states that the actual yield value is a ratio of the number of the ICs or portions of an IC that pass the testing and a total number of ICs or portions of an IC tested. Claim 3 then states that the average yield value is a ratio of the number of the plurality of ICs or portions of an IC that pass the testing and a total number of the plurality of ICs or portions of an IC tested. Thus, when comparing the actual yield value ratio and the average yield value ratio, both utilize here the same mathematical determination because "the *plurality* of ICs" in claim 3 is equivalent to "the ICs" in claim 2 as both refer to plural ICs, and therefore there is some confusion then what distinguishes the average yield value ratio determination from the actual yield value ratio determination. This same type of problem also occurs in claims 12 and 13. Claim 6, line 1, cites "the factor" which lacks antecedent basis. Claim 6, line 2, cites "scaling the actual yield value" which lacks antecedent basis. Claim 8, line 5, cites "sorting the actual yield value into a group from of the plurality of groups" however was this intended to be "sorting the actual yield values into a group from the plurality of groups" ? This same type of problem also occurs in claim 17, line 5. The preamble of claim 11 cites "A method for producing publishable yield information.." however the body of the claim does not particularly point out how the generation of the normalized yield value results in publishable yield information. Claim 18, lines 2-3, cite "the transformed yield value" which lacks antecedent basis. The preamble of claim 19 cites "A system for producing publishable yield information..." however the body of the claim does not particularly point out how the generation of the transformed yield value results in publishable yield information. In addition, the "generate a transformed yield value..."

does not particularly point out how exactly the actual yield value and the average yield value are used to generate a transformed yield value. Claim 19, line 6, cites "..the integrated IC.." which it appears should be "the integrated circuit". Claim 20, line 3, cites "the die" which lacks antecedent basis. The examiner asks the applicant to better claim the limitations cited above. While the examiner understands the intentions of the applicant he feels confusion could be drawn from the limitations cited above. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 1 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Satya et al. (6,751,519).

As per claim 1, Satya et al. (Abstract, col. 3 lines 2-4, col. 8 lines 56-58) disclose "obtaining an actual yield value associated with an integrated circuit...is formed on each one of a plurality of wafers using a semiconductor wafer fabrication process". Satya et al. (Abstract, col. 3 lines 7-10, col. 8 lines 31-33, 64, 66) disclose "determining an average yield value associated with a plurality of ICs....formed on each one of the plurality of wafers using the semiconductor fabrication process". Satya et al. (Abstract, col. 3 lines 4-10, 22-27, col. 8 lines 56-60) disclose "generating a transformed yield value...using the actual yield value and the average yield value".

As per claim 19, Satya et al. (see at least abstract) disclose "a plurality of wafers having an integrated circuit...formed on each one of the plurality of wafers". Satya et al. (Abstract, figures 2, 7, 8, col. 1 lines 29-36) disclose "a tester configured to test the IC or portion of the IC on each one of the plurality of wafers". Satya et al. (Abstract, figure 8, col. 3 lines 2-10, 22-27, col. 8 lines 31-33, 56-60, 64, 66, col. 13 lines 53-56) disclose "a processor configured to obtain an actual yield value ...determine an average yield value...generate a transformed yield value ...using the actual yield value and the average yield value".

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Satya et al. (6,751,519) in view of Yamada et al. (6,842,663).

As per claim 2, Satya et al. (Abstract, figures 2, 7, col. 1 lines 18-24) disclose "testing the IC or portion of an IC formed on each one of the plurality of wafers" and "determining a number of ICs or portions of an IC that pass the testing". It appears though that Satya et al. does not explicitly disclose "wherein the actual yield value is a ratio of the number of the ICs or portions of an IC that pass the testing and a total number of ICs or portions of an IC tested". However, Yamada et al. (col. 9 lines 64-67, col. 10 lines 1, 2) teach this excepted feature. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply the techniques of Yamada et al. to the invention of Satya et al. as specified above because as taught by Yamada et al. (col. 1 lines 45-48) it was usual that a user who ordered the semiconductor devices can not know the number of normal semiconductor devices, which are practically obtained, before the production of all of them is completed.

9. Claims 11-18 are allowed subject to the appropriate correction of the 37 C.F.R. 1.75(a) objections noted in paragraph 4 above.

Claims 3-10 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and subject to the appropriate correction of the 37 C.F.R. 1.75(a) objections noted in paragraph 4 above.

10. The following references are cited as being art of general interest: Simmons (6,265,232) which discloses a yield based, in-line defect sampling method, Sekine (6,289,257) which discloses analyzing correlation for semiconductor chips, Rathei et al. (6,717,431) which disclose a method for semiconductor yield loss calculation, Weng et al. (6,537,834) which disclose that yield signifies the cost and profit of a fabrication process and Atchison et al. (6,393,602) which disclose analyzing the yield losses of semiconductor wafers.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hal D. Wachsman whose telephone number is 571-272-2225. The examiner can normally be reached on Monday to Friday 7:00 A.M. to 4:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc Hoff can be reached on 571-272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hal D Wachsman
Primary Examiner
Art Unit 2857

HW
June 12, 2005